REMARKS

Entry of this response is proper under 37 CFR §1.116, since there are no new claims, claim amendments, or new issues raised herein.

Claims 1-4, 6, 10-15, and 23-30 are all the claims presently pending in the application. Claims 5, 7-9, and 16-22 are canceled.

It is noted that Applicants specifically state that no amendment to any claim herein, if any, should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 1-4, 6, 10-15, and 23-30 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over US Patent Publication 2004/0173812 to Currie, et al., further in view of US Patent Publication 2004/0108559 to Sugii, et al., US Patent Publication 2005/0242395 to Chen et al.

Applicants again traverse this rejection, as revised, in the discussion that follows.

I. THE CLAIMED INVENTION

As described and defined in, for example, claim 1, the present invention is directed to a method of forming a FinFET (Fin Field Effect Transistor) containing a plurality of fins interconnected by fin connectors. At least one localized stressor region is formed within the device, the at least one localized stressor region being located on one of the fin connectors as a region of stressor material filling in an interior portion of the fin connector.

Conventional methods, such as described in paragraphs [0005] through [0007], strain FinFETs by Si or SiGe, but have caused defects, thereby lowering yields.

The claimed invention, on the other hand, provides a localized stressor embedded within the device.

II. THE PRIOR ART REJECTION

In summary, Applicants again respectfully submit that the prior art rejection of record

fails to demonstrate all elements of the claimed invention, since there is no demonstration of providing a localized stressor on the fin connectors of a finFET as a filled-in region on the interior portion of the finFET fin connectors, as required by the independent claims.

In the rejection of record and, more particularly, in the CONCLUSIONS section beginning on page 7 of the latest Office Action, the Examiner is clearly confused as to the components actually shown in Figures 10a-10c and 11 of primary reference Currie. The Examiner points to paragraph [0065] of Currie, alleging that this paragraph describes a finFET having silicon layer 18 as the fins. This characterization is clearly incorrect. Paragraphs [0065-0067] clearly describe a simple MOS transistor with a strained layer 18, not a finFET structure, as alleged by the Examiner:

"*[0065] Referring to FIGS. 10a-10c, a structure 100 may include first and second parallel isolation trench structures 55a, 55b proximate a first source region 102 and a first drain region 104 of a first transistor 106. A first channel region 108 may be disposed between the first source and drain regions 102, 104. First channel region 108 may have a first type of strain. In some embodiments, the first type of strain may be tensile. In other embodiments, the first type of strain may be compressive. At least a portion of the first channel region 108 may be disposed in strained layer 18. A first gate 110 may be disposed above the channel region 108 and between the source and drain regions 102, 104. Gate 110 may be connected to a gate contact 112. A first gate dielectric layer 114 may be formed between gate 110 and channel region 108. First gate 110 and first gate dielectric layer 114 may be collectively referred to as a first gate structure 116. A first and a second sidewall spacer 120, 122 may be formed proximate gate structure 116.*

[0066] First transistor 106 may be formed on layers 13 disposed over substrate 12. As discussed above with reference to FIG. 1a, layers 13 may include, for example, graded layer 14, relaxed layer 16, and strained layer 18. In other embodiments, first transistor 106 may be formed on an SSOI substrate 30, as shown in FIG. 1c. Source region 102, channel region 108, and drain region 104 may be formed in a portion of the SSOI substrate 30, for example, in a portion of strained layer 18.

[0067] Source and drain regions 102, 104 may be formed by, e.g., ion implantation of either n-type or p-type dopants. Gate 110 may be formed of a conductive material, such as doped semiconductor, e.g., polycrystalline Si or polycrystalline SiGe; a metal, e.g., titanium (Ti), tungsten (W), molybdenum (Mo), tantalum (Ta), nickel (Ni), or iridium (Ir); or metallic compounds, e.g., titanium nitride (TiN), titanium silicon nitride (TiSiN), tungsten nitride (WN), tantalum nitride (TaN), tantalum silicide (TaSi), nickel silicide (NiSi), or iridium oxide (IrO.sub.2), that provide an appropriate workfunction. The gate dielectric layer 114 may be formed on strained layer 18 by, for example, growing a SiO.sub.2 layer by thermal oxidation. Alternatively, gate dielectric layer 114 may include a high-k material with a dielectric constant higher than that of SiO.sub.2, such as ZrO.sub.2, Al.sub.2O.sub.3, HfO.sub.2, HfSiON, or HfSiO.sub.4. In some embodiments, gate dielectric layer 114 may be a stacked structure, e.g., a

thin SiO.sub.2 layer capped with a high-k material."

The possible materials for strained layer 18 are discussed in paragraph [0033]:

"[0033] A strained semiconductor layer 18 is disposed over relaxed layer 16. Strained layer 18 may include a semiconductor such as at least one of a group II, a group III, a group IV, a group V, and a group VI element. Strained semiconductor layer 18 may include, for example, Si, Ge, SiGe, GaAs, indium phosphide (InP), and/or zinc selenide (ZnSe). Strained layer 18 may have a starting thickness T.sub.3 of, for example, 50-1000 angstroms (.ANG.). In an embodiment, T.sub.3 may be approximately 200-500 .ANG.. "

From the above recited description, Applicants submit that Currie layer 18 is clearly not described as a silicon layer serving as a fin structure for a finFET transistor, contrary to the Examiner's characterization. Moreover, even if the Examiner were to be given the benefit of the doubt that the strained layer 18 could reasonably be converted into a fin for a finFET, the result would still fail to satisfy the plain meaning of the claim language, since, upon conversion of layer 18 to serve as the fin of a finFET, the entire fin structure would thereby become the stressor. This result does not satisfy the requirement of the final claim limitation that clearly requires that the local stressor be embedded as an internal component region of the fin.

Hence, turning to the clear language of the claims, in Currie there is no teaching or suggestion of: "... said at least one localized stressor region being located on one of said fin connectors as a region of stressor material filling in an interior portion of said fin connector", as required by independent claim 1. Independent claim 14 has similar language.

Therefore, Applicants submit that the rejection of record is deficient as a matter of law and as a matter of fact, since it incorrectly identifies the differences between the claimed invention and primary reference Currie and fails to demonstrate all elements of the claimed invention of even the independent claims.

For this reason alone, all claims are clearly patentable over Currie, and the Examiner is respectfully requested to reconsider and withdraw this rejection.

Relative to the Examiner's attempts to justify the rejection of record based upon the holding in *KSR*, Applicants submit the three cited references, if anything, clearly provide objective evidence of the novelty of the claimed invention, since none of these references demonstrates the concept of providing a local stressor (i.e., within the device) as implemented as a region of stressor material in an interior portion of a component of that device, let alone a

region of stressor material in an interior portion of a fin in a finFET.

Thus, these references arguably might be considered as demonstrating one or more approaches for generating stress in a device, including one or more ways to use local stressors. However, none of the various stressor techniques demonstrate or even suggest using a region of stressor material in an interior portion of a component of that device, let alone a fin of a finFET.

Therefore, if anything, Applicants submit that these references not only do not demonstrate the claimed invention but also that they clearly demonstrate alternative methods to provide stress based on a different approach, thereby providing strong objective evidence that the claimed invention is indeed novel.

Stated slightly differently, the cited references provide alternative methods to achieving stress in a device but do not provide an example of the method of using a stressor region as a localized stressor region within a component of that device. Therefore, the missing element has not even been demonstrated, much less demonstrated as being known in the art as a substitute or improvement in a similar structure, so that the rejection is fundamentally flawed as a matter of law.

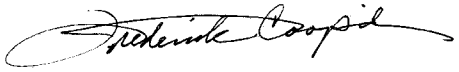
III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-4, 6, 10-15, and 23-30, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,



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